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Design and analysis of novel organic thin film multiplexer

Arun Pratap S. Rathod[1], Pawan K. Mishra[2*]

[1] Department of Electronics and Communication Engineering, Graphic Era Hill University, Dehradun, India
[2] Department of Computer Science & Engineering, Graphic Era Deemed to be University, Dehradun, Uttarakhand, India.
[*]Corresponding author: pawankmishra.cse@geu.ac.in

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Abstract

In recent years a transition from conventional electronic devices based on silicon to organic material based electronic devices has been observed. As the market for flexible and wearable devices has presented greater opportunities and sharp growth, the demand for organic thin film transistor (OTFT) based combinational circuits has increased exponentially. Traditionally such circuits were fabricated through complementary metal oxide semiconductor (CMOS) logic architecture, but due to large number of nodes OTFTs employed in circuit implementation, the overall power consumption, interconnect delay and the chip area of the circuit increases significantly. Organic thin film multiplexer (OTFM) is a novel attempt to redesign an existing multi-transistor combinational logic device like 2:1 Multiplexer in the form of a single multi-layered logical device, while maintaining the dimensions, material composition and fabrication method equivalent to single OTFT (bottom gate bottom contact OTFT). The design and development of the OTFM has been achieved through Silvaco a large ion collider experiment (ATLAS) technology computer-aided design (TCAD) tool while the examination of power and area consumption of the OTFM and equivalent CMOS circuit was accomplished through post layout (physical design) analysis using Cadence Virtuoso exploratory data analysis (EDA) tool. It has been found in this research that the power and chip area consumption of proposed OTFM is lower than that of CMOS logic based 2:1 Multiplexer by 90% and 95% (approx.) respectively, while operating under same voltage regime for implementing identical logical functions.

Keywords: Multiplexer; OTFT; Organic electronics; Thin films; CMOS; OTFM.

1. Introduction

Organic electronics has come into vogue more prominently in the preceding couple of decades, due to the integral material flexibility, elementary and inexpensive techniques of fabrication. Also, the advent of organic semiconductors with greater charge mobility has also contributed to the rise of organic devices [1]. Contemporarily, organic electronic devices are largely concentrated in the domain of radio frequency identification (RFID) tags [2], Organic light emitting diode (OLED) also known as organic light emitting diode for display applications and to some extent to organic sensors and logic circuits built from organic thin film transistor (OTFTs) [3]. Although, over the years the charge transportation inside organic semiconductors have enriched significantly [4] but still comparatively silicon has proven to be the superior semiconductor material for computational applications. As a result, continuous work has been made over the years to improve the performance of organic transistors in particular and organic electronic devices in general [1, 5].

Combinational logic circuits are an integral part of an electronic device that has computational functionality [6]. With growing demand for smart wearables powered by organic electronic technology, the need for efficient combinational logic circuits has increased exponentially. Such circuits are the result of a logical interconnection of different organic thin film transistors designed to generate the desired output. Complementary metal oxide semiconductor (CMOS) logic architecture is widely used to design complementary logic circuits like 2:1 Multiplexer (Mux). Multiplexer is a key component in present day optical communication systems as highlighted

by Gelkop et. al. and Menahem et. al. [7-9]. Researchers like Gindi et. al explored the applications of multiplexing and demultiplexing techniques in slot-waveguide structures [10].

Moreover, multiplexers are also employed in optimization of thermo-optic phase shifter heaters and minimizing multimode interference in data centres making it an indispensable part of digital communication systems [11-13]. However, CMOS design architecture commissions a large number of transistor OTFTs nodes in order to generate the required logical output. For instance, 20 OTFTs are required to implement 2:1 Multiplexer built using the CMOS logic design framework. Consequently, higher number of transistors in the circuits result in high magnitude of overall power consumption which is evident from Eq. (1) and (2). The chip area (circuit size) required to implement such circuits is also enormous given the larger size of OTFTs. Also, the greater interconnections nodes in the circuit further contribute to the overall propagation delay in the circuit [14].

$$P_{avg} = (\Sigma \alpha_{Ti}. C_i. V_i). V_{DD}. f_{clk} \quad (1)$$

$$P_{avg} = (C_{load}). V_{DD}^2. f_{clk} \quad (2)$$

Here node transition factor is denoted by α_{Ti}, C_i implies capacitance of parasitic nature attributed to each node, V_i is node voltage, V_{DD} represent voltage supply, C_{load} is lumped capacitance of circuit and clock-frequency is denoted by f_{clk}.

As shown in Eq. 1 and 2 that the average dynamic power dissipation is the amount of power consumption required by the transistors or OTFTs while switching between the states viz. '0' and '1' states. This switching occurs as a consequence of charging and discharging of load capacitances taking place in the circuit. The transition or switching activity factor α represents the possibility of a transistor connected in the circuit to switch between low (0) and high (1) per clock cycle. This transition factor is associated with each transistor operating in the circuit and its summation is represented by α_{Ti}. It is worth noting here that the transition factor is directly proportional to average power consumption of the circuit, and it increases with the number of transistors or nodes in the circuit. The C_{load} is the cumulative capacitance generated at the output terminal of a transistor comprising interconnect capacitance, parasitic capacitances and intrinsic gate capacitance. Greater the load capacitance more power will be consumed per switch. The supply voltage V_{DD} is another parameter responsible for scaling power dissipation in a circuit. Power consumption increases quadratically with rise in voltage, implying that a small reduction in the supply voltage can significantly reduce the power dissipation. Finally, the operating frequency represented by f_{clk} is responsible for switching events taking place per unit time. Higher the frequency, greater will be the switching events (charging and discharging of load capacitance) resulting in greater average power dissipation.

Therefore, it is important to optimize these parameters viz. α_{Ti}, C_{load}, V_{DD}, and f_{clk} for effective reduction in average power consumption. Hence, in this study an effort has been made to reduce two of these parameters i.e., transition factor and cumulative load capacitance by reducing the overall number of transistors in the circuit (2:1 multiplexer) while maintaining the uniformity and functional stability of the combinational circuit architecture. The proposed single stacked multi-layered Organic Thin Film Multiplexer (OTFM) device with tri-input and single output is a novel attempt to redesign the existing multi-transistor combinational logic device 2:1 Multiplexer into a compact integrated single multi-layered device devoid of interconnected nodes. The physical dimensions, material composition and working principal of the proposed OTFM are maintained similar to a single OTFT (bottom gate bottom contact OTFT) [15, 16], but its performance and logical output are identical to a 2:1 Mux combinational logic circuit comprised of 20 single gate OTFTs [17]. Since the proposed OTFM is comprised of only one OTFT (dimensionally), it reduces the chip area drastically [18-20]. Moreover, the interconnecting nodes, power consumption and overall transistors required to design a conventional 2:1 Multiplexer are also minimised.

2. Materials and methods

Design and validation of OTFM and corresponding CMOS designed based 2:1 Multiplexer is accomplished through computer aided design software Silvaco technology computer-aided design (TCAD) a large ion collider experiment (ATLAS) simulator [21]. Furthermore, the prediction of results lying within the boundary limits has been calculated through mobility model proposed by Poole-Frenkel [22-23]. expressed.

$$\mu(E) = \mu_0 \, exp\left[-\frac{\Delta}{kT} + \left(\frac{\beta}{kT} - \gamma\right)\right] \quad (3)$$

Here k, μ(E), μo, T, and E represents the Boltzmann constant, field dependent mobility, zero field mobility, temperature, and electric field respectively. The parameters like hole Pool-Frenkel factor and zero-field activation energy are indicated through Δ and β respectively and fitting parameter is represented by γ in the equation.

calculation of the charge conduction generated through field induced thermal excitation of trapped charge carriers is achieved through this model. Localization of charge carriers around the traps results in reduction of drain current inside the low field region [24-25].

Silvaco TCAD ATLAS software is a comprehensive tool used for the design and analysis of various semiconductor devices, including OTFTs. It provides a powerful platform for simulating and optimizing the performance of OTFTs across different performance parameters [26]. TCAD ATLAS utilizes advanced modeling techniques and numerical methods to accurately capture the behavior of these devices under various operating conditions. The Poole-Frenkel mobility model, integrated into Silvaco TCAD ATLAS, is an essential component for analyzing the performance of OTFTs [21]. The Poole-Frenkel model describes the mobility attributed to charge carriers residing inside organic materials based on the Poole-Frenkel effect. This effect is a phenomenon observed in certain materials where the presence of electric fields leads to an increase in the effective mobility of charge carriers, resulting in enhanced conductivity. By incorporating the Poole-Frenkel mobility model into the simulations performed in TCAD ATLAS, it becomes possible to accurately predict the electrical behavior and performance of OTFTs. The model takes into account factors such as trap densities, electric field effects, and the interaction between the localized states and charge carriers within the organic semiconductor. After the completion simulation of OTFT structures using TCAD ATLAS and obtaining their properties and dimensions, the next step is to import this information into Cadence Virtuoso. Cadence Virtuoso is a widely used electronic design automation (EDA) software suite that provides a comprehensive platform for designing and simulating complex integrated circuits. It offers a user-friendly interface and a wide range of features to facilitate the design, layout, and analysis of electronic circuits. This integration between the two software tools enables designers to leverage the optimized OTFT parameters in the design of more complex circuits, such as 2:1 multiplexer [17]. A comprehensive analysis is conducted to evaluate the performance of the multiplexers using OTFTs [6]. This involves conducting simulations and assessing various parameters related with performance of OTFTs, viz. propagation delay, power-delay product, and power consumption, under different input patterns and operating conditions. Moreover, key metrics like chip area consumption and power dissipation were also considered in the analysis. Chip area consumption refers to the physical space occupied by the circuit on the integrated chip, and minimizing this space is crucial for achieving compact and densely packed designs. Power dissipation represents the amount of power consumed by the circuit during operation and is a critical factor for energy efficiency and overall system performance. By comparing the results obtained from different multiplexer designs, valuable insights can be gained regarding their performance trade-offs and suitability for specific applications.

A 2:1 multiplexer is one of the fundamental components in digital circuits that allows the selection of one of two input signals to be routed to a single output. By utilizing OTFTs in the design of the multiplexer, the circuit can benefit from the inherent properties of organic materials, such as flexibility, low power consumption, and potentially lower manufacturing costs. The demand for organic transistor-based combinational circuits has seen significant growth in recent years [7]. These circuits are constructed by interconnecting various organic transistors like bottom gate bottom contact (BGBC) OTFT in a logical design to achieve the desired output. Figure 1 illustrates a conventional BGBC OTFT, whereas in Figure. 2, 20 BGBC OTFTs are connected in a CMOS logic architecture to design a functional Multiplexer (2:1 Mux) with three inputs and one output [6]. As these circuits employ a large number of transistors, the overall power consumption and chip area increase. Moreover, the extensive interconnections (nodes) in the circuit contribute to increased data delay from input to output.

(A)

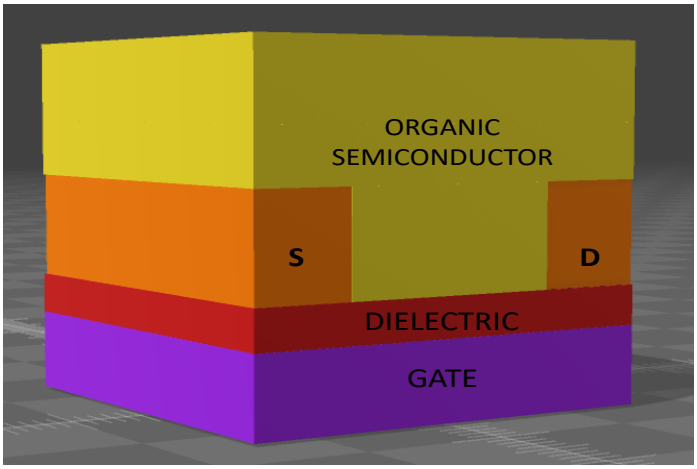

Figure 1 (A) 3-D structure of BGBC OTFT; (B) 2-D simulated structure of BGBC OTFT.

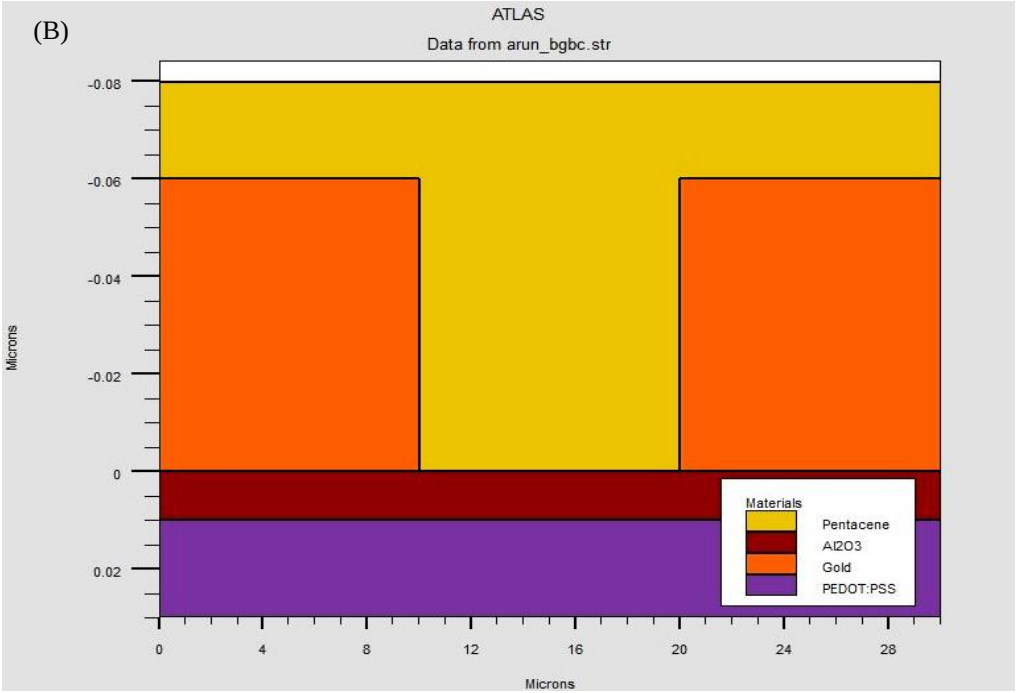

Figure 1 (cont.) (A) 3-D structure of BGBC OTFT; (B) 2-D simulated structure of BGBC OTFT.

A multiplexer functions as a data selector, choosing among various incoming digital or analog input signals to transfer the desired input signal to the designated output data port. This selection of the input data line (A and B) is facilitated by another set of input lines called select lines (S). These select lines isolate the data from other input lines, ensuring that only the data of the selected input reaches the output port (Y). The significance of the multiplexer lies in its ability to allow multiple input signals to share a single resource or nodal device.

A typical CMOS-based 2:1 multiplexer designed with complementary topography utilizes 20 OTFTs, comprising 10 N-type OTFTs and 10 P-type OTFTs. The circuit representation of the CMOS logic design-based 2:1 multiplexer is presented in Figure 2. The OTFTs used in this design are of the BGBC type, with a channel length of 10μm, a width of 100μm, and an organic semiconductor layer thickness of 80 nm. Therefore, the methodology outlined here highlights the use of Silvaco TCAD ATLAS software for the design and analysis of OTFTs, incorporating the Poole-Frenkel mobility model. The properties and dimensions of the simulated OTFTs are then imported into Cadence Virtuoso software for the analysis of multiplexers circuits. The resulting circuits were compared in terms of chip area consumption, power dissipation, and other performance parameters.

The estimation of power dissipation in the competing circuits is achieved through Post Layout Power Analysis, one of the most accurate power estimation techniques using layout or physical design of a circuit. Through this method the power consumption of transistors as well as parasitic effects caused interconnects by interconnected are also calculated. The process is initiated by performing design rule check (DRC) and layout vs schematic (L VS) checks for ensuring the accuracy and validity of the physical layout. Thereafter extraction of parasitic capacitances along with parasitic resistances, and inductances in interconnections are accounted for. This extracted parasitic data along with switching activity data of nodes (transistors) is imported in the circuit simulation tool and real test vectors are applied imitating actual input signals and comprehensive circuit simulation is performed to observe the transient behavior of the circuit. The output waveforms thus generated provide quantitative analysis of average power dissipation and power hotspots in the circuit utilizing the data representing transistor switching activity, parasitic capacitances, leakage current etc. [27].

Similarly, to calculate the chip area the analysis of physical design is done by transforming a gate level design (netlist) into a physical layout ready to be fabricated on the silicon chip. The process of total circuit area calculation is initiated after the completion of processes like floor planning, placement and routing. During the total area calculation of circuit parameters like standard cell utilization, white space, routing overhead, die size are analyzed in totality. The standard cell utilization is the ratio of total area occupied by standard cells to the total area of the floorplan. Higher utilizations imply the chip area is used efficiently but may lead to congestion in the interconnections, the white space represents unused area on the chip which is reserved for channel routing, thermal management, and further modifications. Too much white spaces indicate poor efficiency in area consumption. The routing overhead and die size provide insight into the congestion in the routing layers and overall device size incorporating routing tracks, standard cells, power rails, and other overhead area consumptions respectively.

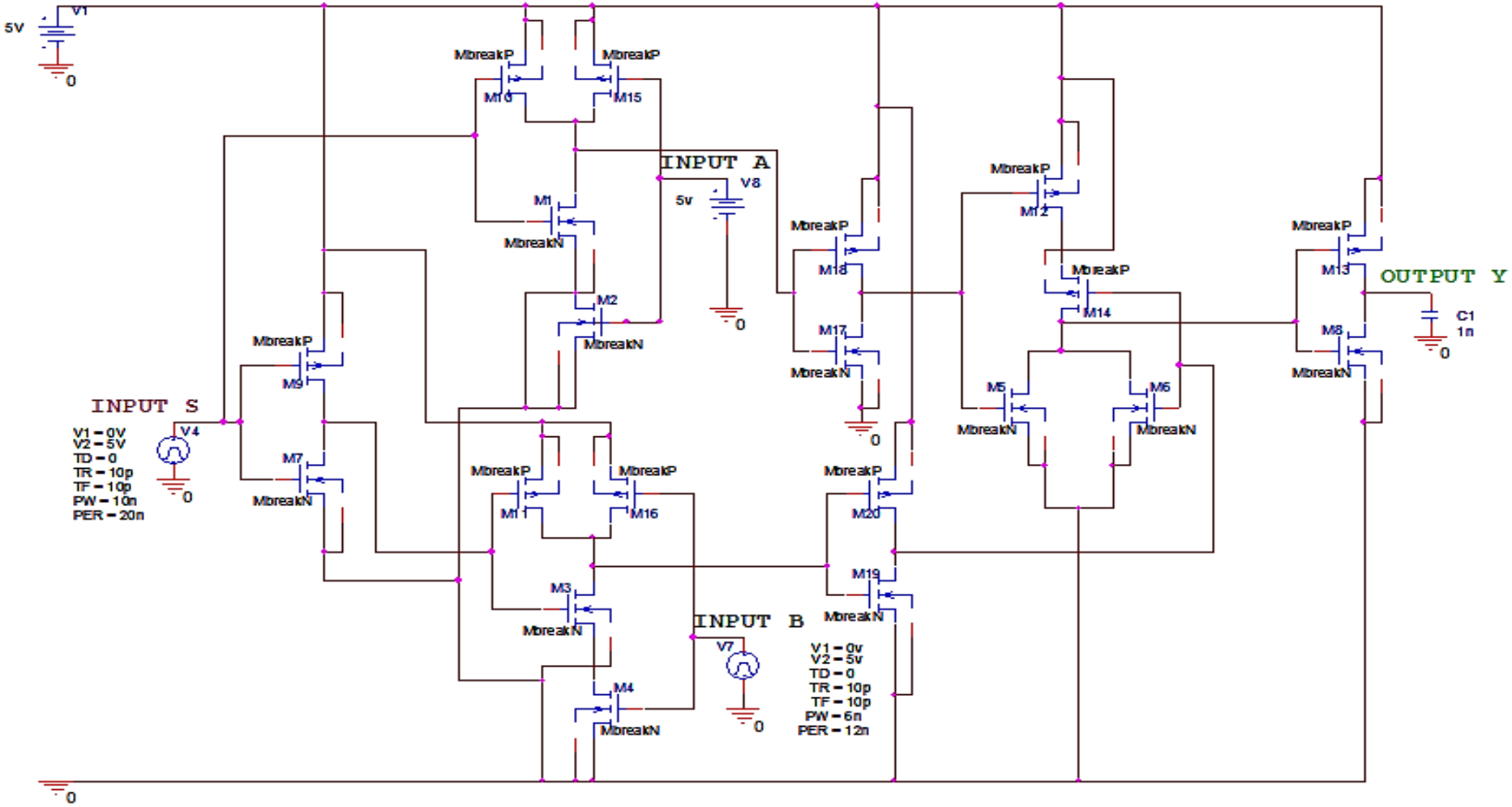

Figure 2 Schematic representation of simulated 2:1 multiplexer designed using BGBC OTFT via CMOS logic design.

Using these parameters, the final area report is generated by the electronic (physical) design tool [27]. This report includes outcomes like the Core Area, the actual area used for logic implementation using transistor architecture and routing; Total Die Area, it represents the core area in addition to Input/Output pads, additional overhead spaces. The report also highlights the percentage of the total area occupied by standard cells as Cell Utilization Rate and congestion hotspots in routing and interconnections as Routing Congestion Metrics.

To perform the comparative study of the CMOS architecture based 2:1 organic multiplexer and OTFM device both devices are simulated independently, and their performance parameters are recorded using the above explained methodology. The average power dissipation is calculated for the circuits and compared objectively. Similarly, to calculate comparative area consumption of both circuits, the core area' is calculated and studied relatively to determine percentage change. Through this integrated approach, a deeper understanding of the performance characteristics and potential applications of OTFT-based circuits is developed, and better comparison of performance characteristics could be performed.

3. Results and Discussion

The proposed OTFM is a multi-layered single stacked combinational logic device capable of performing logical operations of a 2:1 Multiplexer. It consists of two organic semiconductor layers: a top layer (p-type) and a bottom layer (n-type). The oscillator (OSC) layer facilitates the formation of conduction channel within its dimensions providing the charge carriers a conducting path and assisting the formation of drain current inside the device. In addition, the OTFM also incorporates two gate dielectric layers: one on the top and one at the bottom of gate electrode creating barrier between the central gate and the respective organic semiconductor layers. This is important as it helps in prevent in charge migration and generates gate capacitance in the device. The device features a single gate placed at the center of the device between the top and bottom gate dielectrics. When the desired potential difference is applied between source and gate electrode, the charge carriers tend to get accumulated in the channel region of both OSC layers which is essential for the generation of drain current. Furthermore, a pair of source and drain electrodes are positioned above top OSC layer and another pair above substrate encapsulated by bottom OSC layer, as depicted in Figure 3(A) and 3(B). On applying suitable potential difference between source and drain electrodes the accumulated charge carriers in the channel regions start moving towards respective drain electrodes forming the drain current. These operational principles are used in design and validation of the OTFM as a single device capable of functioning as an independent 2:1 multiplexer.

(A) (B)

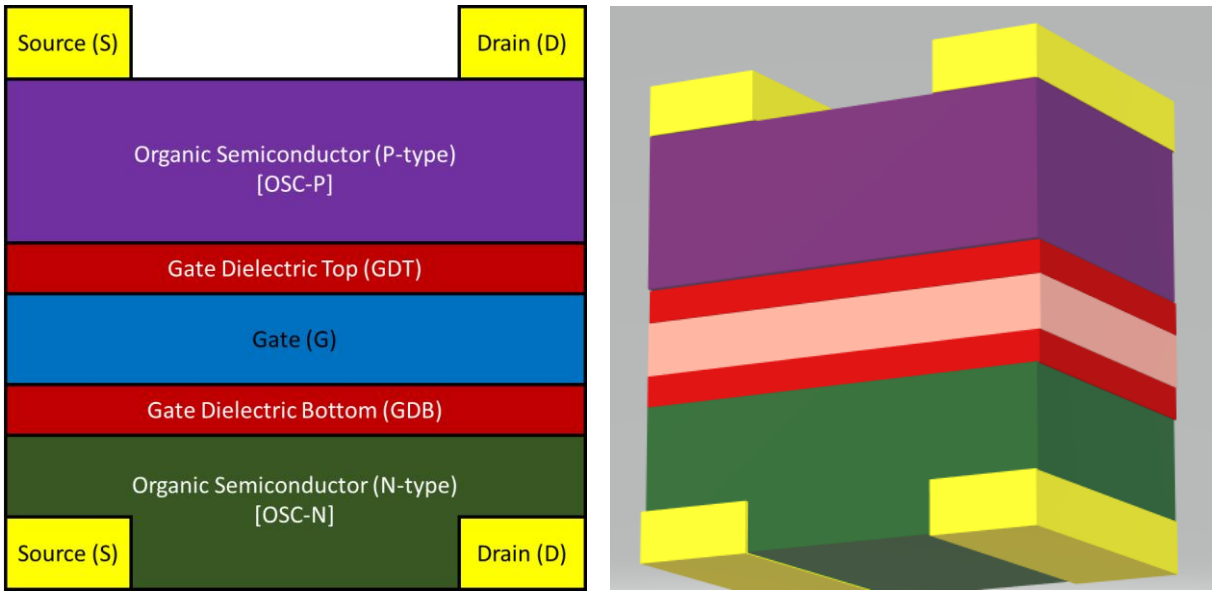

Figure 3 (A) 2-D & (B) 3-D representation of OTFM with corresponding material layers arrangement; (C) Organic thin film multiplexer as 2:1 Multiplexer with 3 input and 1 output port.

(C)

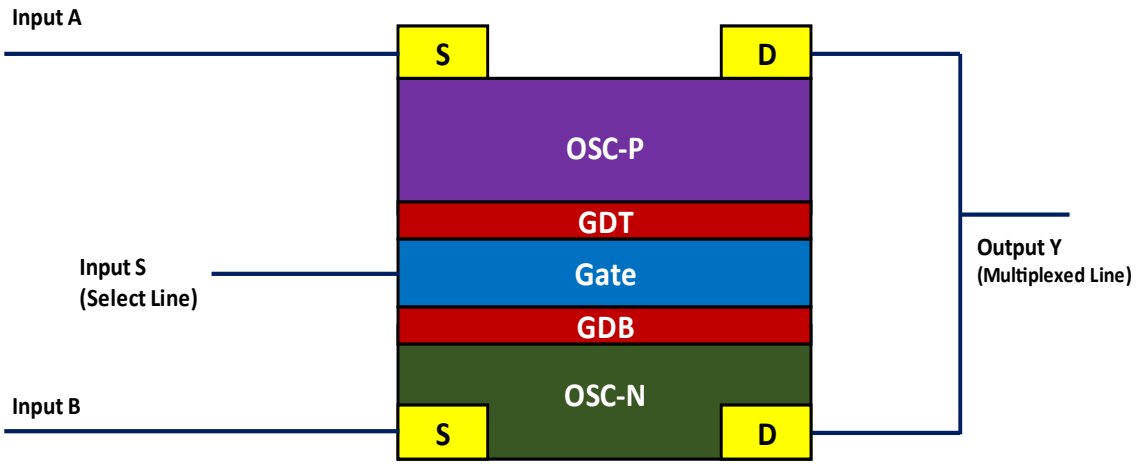

Figure 3 (cont.) (A) 2-D & (B) 3-D representation of OTFM with corresponding material layers arrangement; (C) Organic thin film multiplexer as 2:1 Multiplexer with 3 input and 1 port output.

The fabrication of proposed OTFM as elucidated in Figure 4 is initiated on a plastic or glass substrate as it has somewhat inverted staggered architecture [28]. In second step, twin bottom electrodes viz. source and drain (Au) are deposited through a shadow masking process with a thickness of 20 nm using physical vapour deposition technique. Before initiating the step 3, electrode surface treatment' is done as a precursor to deposition bottom semiconductor layer over the electrodes for optimum grain growth as it is important for achieving greater mobility in the bottom-contact field effect devices. As a result of electrode surface treatment, using a self-assembled monolayer (SAM) of hexadecanethiol, a larger semiconductor grain growth on electrodes with greater carrier mobility is attained [29]. Thereafter, the mask alignment is manually done with aid of an optical microscope. In the next step a 50nm thick n-type (fullerene) OSC (bottom) layer is deposited in vacuum and temperature-gradient sublimation is done purifying the deposited layer [30]. A 10nm thin film of Al_2O_3, Aluminium oxide was deposited as dielectric material, above the bottom OSC through atomic layer deposition technique (ALD).

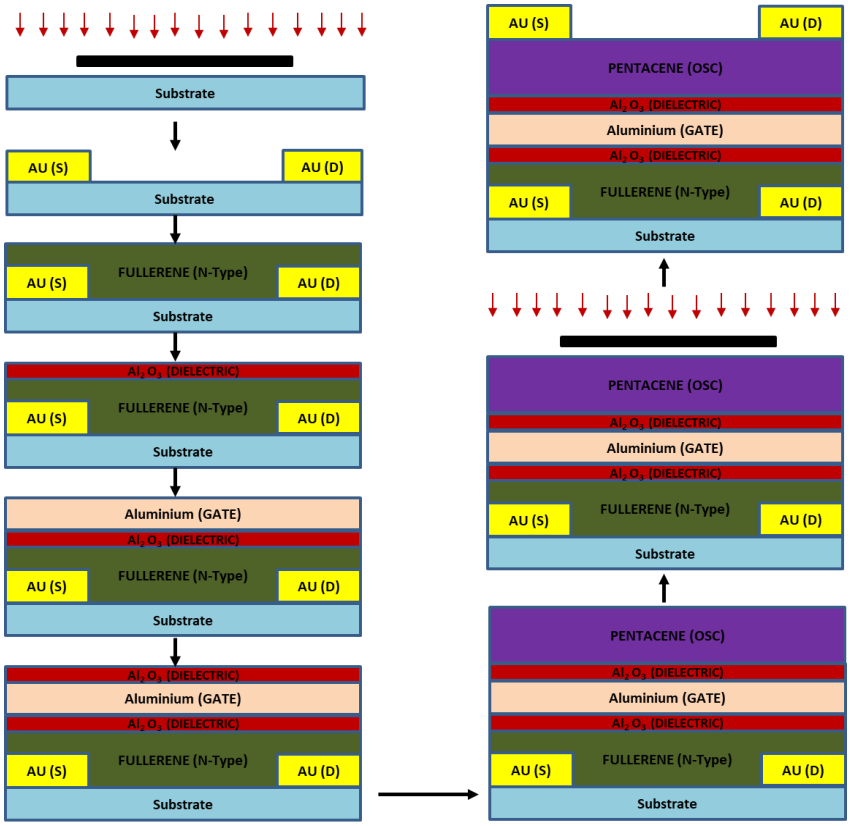

Figure 4 Fabrication flow of proposed OTFM.

The ALD is a categorised as high precision deposition technique offering precise control over the thickness of deposited layers at relatively moderate temperatures (often <150°C) minimizing any damage to the OSC layer. ALD technique also provides excellent conformality, minimising defects in dielectric thin films with higher resistivity and reasonable barrier properties [31]. The central gate electrode (Al) is deposited in the consequent step, through vapour deposition technique [30]. The fabrication of aluminium oxide layer of 10nm above central gate is achieved after treating the gate electrode with oxygen plasma. In the penultimate step an p-type OSC (pentacene) layer with 60nm thickness is deposited in vacuum conditions, forming top OSC layer and temperature-gradient sublimation is used for OSC layer purification. Finally, a pair of gold electrodes (top source and drain) are deposited using physical vapour deposition via shadow masking completing the fabrication process [30].

The working principle of the OTFM can be understood by dividing its structure into two mutually exclusive organic thin film transistors based on their mode of operation, as shown in Figure 5 (A) and 5 (B). These OTFTs share a common gate and can be represented as two OTFTs connected through the gate, as illustrated in Figure 3(C). The top OTFT is of P-type, while the bottom OTFT is of N-type. The gate is connected to the input select line 'S'. When a high input voltage (5V, Logic '1') is applied at the gate, the bottom OTFT (N-type) becomes operational as the conduction channel becomes operational, and input B is transmitted to the output port 'out' in the form of drain current. Similarly, when a low input voltage (0V, Logic '0') is applied at the gate, the top OTFT (P-type) becomes operational implying that its conduction channel is now operational, and input A is transmitted to the output port 'out' as the drain current has started moving from source to drain terminal. The logical output at the output port 'out' oscillates between input 'A' and input 'B' depending on the logical value provided at the select line 'S'. This behaviour is achieved through the functioning of the OTFTs and their corresponding electrical characteristics. To further develop into the working mechanism of the OTFM, it is essential to understand the operation of the individual OTFTs within the device. OTFTs are the transistors that operate under the influence electric field, where the conductivity of the organic semiconductor layer is moderated the electric field applied through gate electrode [21, 22].

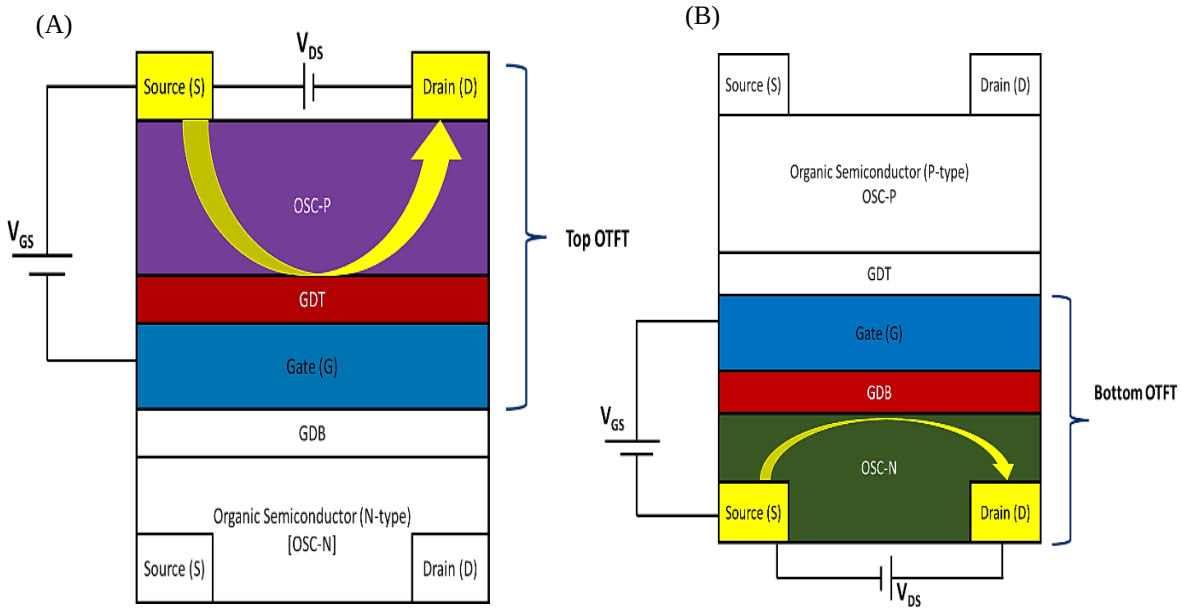

Figure 5 (A) Top OTFT functioning mode of OTFM. (B) Bottom OTFT functioning mode of OTFM.

Table 1 Different physical dimensions & materials used in analysis of multi-layered OTFM.

Material Layers	Physical Dimensions
Length of Channel	10 µm
Width of Channel	100 µm
OSC layer Top (thickness and material)	50nm, Pentacene
OSC layer Bottom (thickness and material)	50nm, Fullerene
D and S electrode (thickness and material)	40nm, Gold [20nm top + 20nm bottom]
Gate electrode (thickness and material)	25nm, Aluminium
Gate dielectric (thickness and material)	30nm, Al_2O_3, [15nm top + 15nm bottom]

The conductivity modulation is achieved by altering the number of charge carriers (electrons or holes) in the organic semiconductor layer [23], thereby influencing the current flow through the transistor [24]. The dimensions and the material composition of the organic thin film multiplexer used in the simulation and subsequent analysis of the device are presented in Table 1. After successfully generating the structure of OTFM, the device dimensions and material properties were exported to EDA software for utilizing the device as circuit component. Thereon, the device was implemented as standalone 2:1 multiplexer and performed substantially well to achieve the desired output. The circuit simulation schematic of OTFM is elucidated in Figure 6 (A) and its schematic description to establish the analogy with the structure of OTFM (as displayed in Figure 3(C)) is presented in Figure 5 (B).

In summary, the proposed OTFM comprised of two organic semiconductor layers, two gate dielectric layers, and a single gate stationed between the two. Drain and Source electrodes are placed above the top OSC layer and inside bottom OSC layer to facilitate the conduction of charges inside conduction channel region. It functions as a 2:1 multiplexer by utilizing the unique architecture of OTFM that allow two mutually exclusive OTFTs to exist in the same structure. The activation of P-type OTFT is initiated on the application of low input voltage at the gate that act as a select line (S), transmitting input A to the output Y, on the other hand activation of the N-type OTFT is attributed to application of a high input voltage to gate terminal, transmitting input B to output port Y. The logical output at the output port 'Y' oscillates between inputs A and B based on the logical value provided at the select line 'S'.

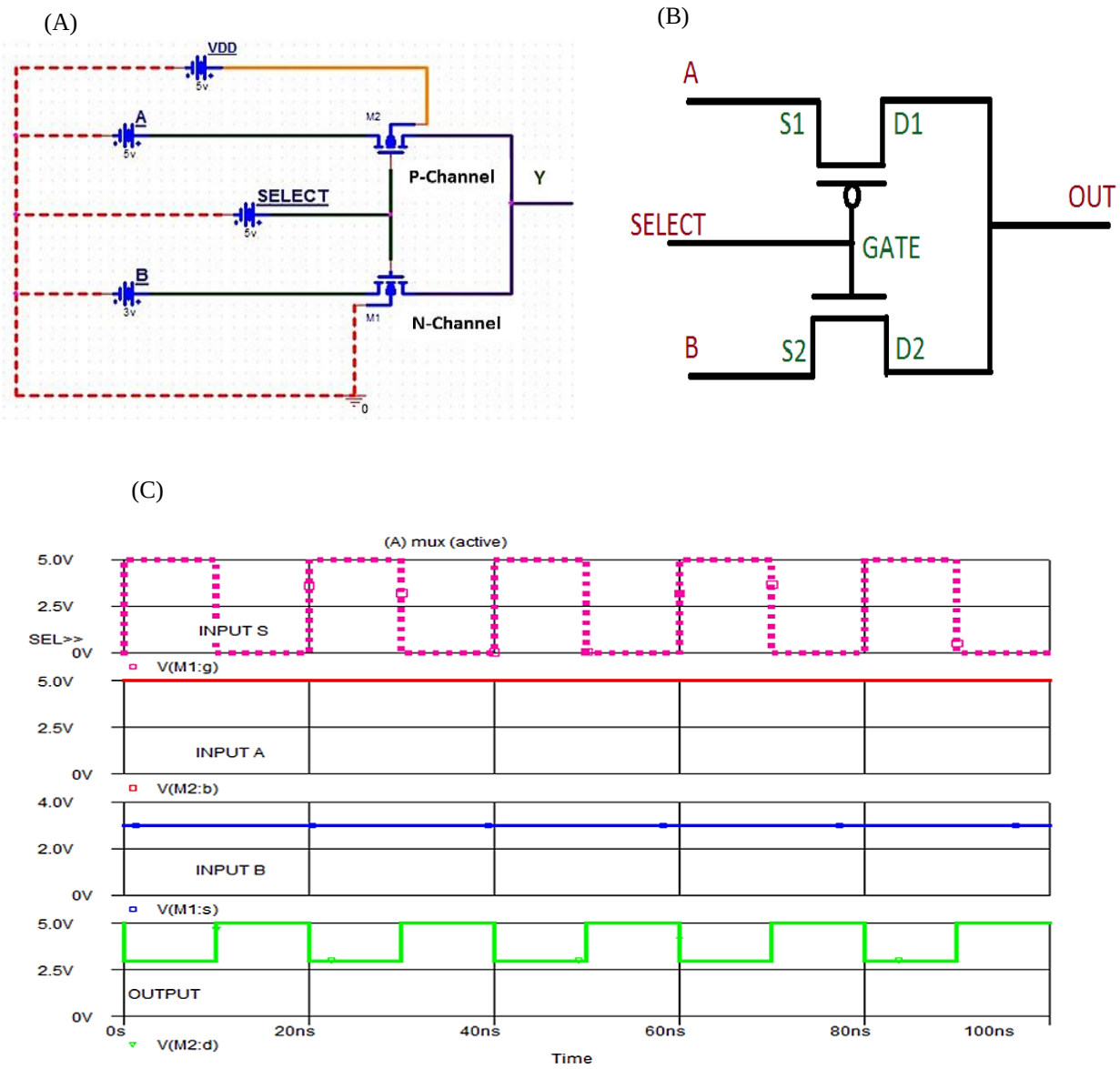

Figure 6 (A) Circuit representation of OTFM; (B) Schematic diagram of OTFM comprised of both Top and Bottom OTFT; (C) Logic output of 2:1 Multiplexer implemented through OFTM, where input A is 5V and input B is 2.5V and S is select line.

The results presented in Table 2 show a performance comparison between the OTFM-based multiplexer and the CMOS-OTFT-based multiplexer. The results clearly indicate several advantages of the OTFM design over the conventional CMOS-OTFT design in terms of size consumption, power consumption, number of transistors, interconnections, and output voltage levels. To begin with, the overall size consumption of the OTFM-based 2:1 multiplexer is significantly more economical compared to the CMOS-OTFT-based multiplexer. This means that the OTFM design requires less chip area to implement the same functionality, potentially enhancing cost effectiveness and increased integration density.

Table 2 Different performance parameters values obtained after the analysis of CMOS-OTFT circuit and OTFM circuit based 2:1 multiplexer.

Performance Parameters	OTFM	CMOS-OTFT Architecture
Input voltage level (V)	3 to 5	0 to 5
Number of OTFTs	1 (operates as n-type and p-type OTFT alternately)	20
Power consumption (µW)	115	1200
Chip area consumption (μm^2)	1100	22000 (approx.)
Interconnections	Minimized	Maximized

The chip area consumption (core area) of OTFM is found to be 1100 μm^2, which is significantly less than the 22000 μm^2 (approx.) chip area (core area) consumed for CMOS-OTFT, clearly illustrating the advantage in terms of size. The reduction in size consumption is validated by the circuit representation shown in Figure 2 and Figure 6 (A). Moreover, the power consumption of the OTFM-based 2:1 multiplexer is considerably lower compared to the CMOS-OTFT-based design. Lower power consumption is highly desirable in electronic circuits as it leads to improved energy efficiency and reduced heat dissipation. The power consumption values provided in Table 2 state 115 µW consumption for OTFM and 1200 µW power consumption for CMOS-OTFT. This demonstrates the significant power-saving potential of OTFM design. This reduction in power consumption can be attributed to the optimized device characteristics and operation of the OTFTs in the OTFM design. The logical output of the OFTM based 2:1 multiplexer is presented in Figure 6 (C), which validates its functionality and operational reliability. Furthermore, the number of transistors is minimized in the OTFM-based multiplexer. Minimizing the number of transistors is advantageous as it simplifies the circuit design, reduces complexity, and improves reliability. The OTFM design requires only single OTFTs, whereas the CMOS-OTFT architecture employs twenty OTFTs, as indicated in Table 2. This significant reduction in the number of transistors contributes to lower fabrication costs and enhanced circuit performance. In addition, the interconnections in the OTFM-based multiplexer are also minimized compared to the CMOS-OTFT-based design. Minimizing interconnections offers several benefits, including reduced signal delay, improved signal integrity, and lower susceptibility to noise and interference. The OTFM design effectively minimizes interconnections, resulting in improved circuit performance. This advantage is highlighted in Figure 5(A), where the OTFM design is show "minimized" interconnections.

Lastly, the output voltage levels of the OTFM-based multiplexer can operate efficiently for intermediary voltage ranges of 3 to 5 volts, whereas the CMOS-OTFT architecture could only work in the full sweep voltage ranges (starting from 0V) like 0 to 5 volts. The output voltage levels are important for compatibility with other circuitry and ensuring proper signal transmission. The specified voltage ranges for both designs cater to different operational requirements and can be adjusted accordingly.

To summarize, the performance comparison between the OTFM-based multiplexer and the CMOS-OTFT-based multiplexer demonstrates the numerous advantages of the OTFM design. These advantages include reduced size consumption, lower power consumption, minimized number of transistors and interconnections, and compatible output voltage levels. These benefits stem from the unique characteristics and optimized operation of OTFTs in the OTFM design. By leveraging these advantages, the OTFM-based multiplexer offers a more efficient and cost-effective solution for implementing 2:1 multiplexing functionality in organic electronics applications.

4. Conclusions

The research paper highlights the superiority of the OTFM-based multiplexer over the CMOS-OTFT multiplexer in terms of various performance parameters. The OTFM design achieves a reduction in size consumption by an impressive 95% approx. This substantial decrease translates into increased integration density, potential cost savings and compact circuit layout. The power consumption of the OTFM-based multiplexer is approximately 90% lower, compared to the CMOS-OTFT architecture. Decrement in power consumption

improves energy efficiency and reduces heat dissipation, for development of sustainable and power-efficient electronic systems. The OTFM design minimizes the transistor count and interconnections by 90% compared to the CMOS-OTFT architecture.

5. Conflict of Interest

The authors declare that they have no conflict of interest.

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