Development of A Data Acquisition Board for Measuring HDD signals

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Abstract

The rapid improvement of digital technology leads to its frequent uses in monitoring systems. Data from external world is read, processed, and, eventually, output by a digital system. This paper presents development of a data acquisition board which communicates with computers via USB port. In the same board, a Low Noise Amplifier (LNA) will be incorporated in order to make this board suitable for measuring hard disk reader signals. The system is composed of a low noise amplifier, an Analog to Digital Converter (ADC), a controller unit and USB controller. The LNA has a gain of 10 V/V, and a bandwidth of 300 MHz. Its 12-bit ADC samples an input at 240 MSPS, 70 microseconds consecutively every 100 millisecond cycle.

Keywords: Data Acquisition; Low Noise Amplifier; Analog to Digital Converter; Hard disk drive

Introduction

The present storage technology is developed for high-density data storage, and high-speed recording. Hard disk is an essential component that is used for data storage in a computer system. The electric signal which occurs at the read/write head of hard disk has a wide bandwidth but its amplitude is very small. Digital signal processing of such signal for failure analysis requires very high sampling rate data acquisition board and low noise amplifier (LNA). Both devices are high cost, a few hundred thousand Bath in the market. This is because of their general purposes and low-volume market. Hence, this paper will present development of a data acquisition board, which communicates with PC via USB port. In the same board, LNA will be incorporated in order to make this board suitable for measuring signal from HDD readers. This board is designed to support the preamplifier head signal amplitude ±100 mV from HSA (Head Stack Assembly) read channel output, and must sampling at 240MSPS with 12-bit resolution, 70±s continuously, and resampling every 100 ms.

USB Interface Basic Concept (Jan, 2005).

USB is a serial bus conceived for an easy and expandable way for connecting peripherals to PC. The USB divides in 2 parts: USB host controller and USB peripheral. The host controller is usually embedded in the mother board on PC. USB controller

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can accommodate up to 127 peripherals. However, only one device at a time can communicate with a host controller.

The host and its devices each have defined responsibilities. The host's duties are communicate with USB devices, computer need hardware and software support that enable the computer to function as a USB host. The hardware consists of a USB host controller and a root hub with one or more USB ports. The software support is an operating system that provides a mechanism for drivers to communicate with the USB hardware. The host needs to know what devices are on the bus and the capabilities of each device. Each device attached to the host must also have device driver that enables PC applications to communicate with it. Applications program do not have to worry about the USB specific details of communicating with devices. All application has to do is send and receive data using standard operating system functions that are accessible from just about all programming languages. The task which the host need to perform is detect device, manage data flow, error checking, provide power and exchange data with peripherals.

The peripherals' duties are a mirror of the host's. When the host initiates communication, the peripherals must respond. But peripherals also have duties that are unique. A peripheral can't begin USB communications on its own. It must wait and respond to a communication from the host. The USB controller in the peripheral handles many of the device's responsibilities in hardware. The amount of support required by device firmware varies with the chip. The peripheral must detect communications directed on the chip, respond to standard requests error check, manage power, and exchange data with the host.

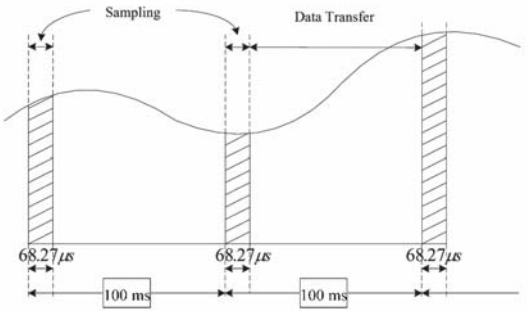

Figure 1. The sampling technique and data transfer

Samples technique

The data acquisition board has an ADC for converting analog to digital signal. An ADC has sampling rate of 240 MSPS in 12-bit resolution. The digital data is recorded in a block memory contained in a FPGA (Field Programmable Gate Array). The size of memory is 16384x12 bits, which can stores up to 68.27±s data at a time. Sampling occurs every 100 ms period. The timing for sampling data and transferring it to PC is shown in Figure 1.

Data Acquisition Board

The data acquisition board consists of an LNA, an ADC, a clock generator, a controller unit and a USB controller. The input of the system is an analog signal from an HDD reader. The signal level is amplified by the LNA to improve signal to quantization noise ratio. The clock generator is used for configuration sampling rate of ADC and clock source of an FPGA (Field Programmable Gate Array). Digital output of the ADC is an input to the controller unit. The controller unit is synthesized in an FPGA, which has an interface with the USB controller. The block diagram of data acquisition board is shown in Figure 2.

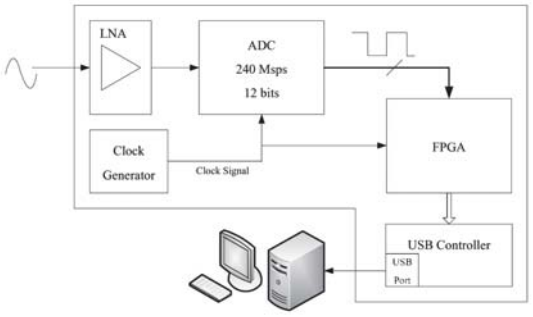

Figure 2. The block diagram of data acquisition board

A. Low Noise Amplifier

Amplifier is designed to have 10 V/V gain. It is implemented by Max4107 (Maxim, 2007) because of its low voltage noise. Its input/output impedance is 50W.

B. Clock Generator

The ADC requires its input clock for sampling at 240MHz. We use CDC5801A (Texas Instrument, 2006), which is a frequency multiplier chip and 60 MHz oscillator as an input to its chip. We set multiplier to 4, hence we get 240MHz from clock generator output.

C. Analog to Digital Converter

The system requires an ADC which has 240 MSPS sampling rate at 12-bit resolution. LTC2242-12 (Linear Technology, 2006) is selected for this paper. It made by Linear Technology. It is designed for digitizing high frequency, wide dynamic range signals. The digital from output can be either differential LVDS or single-ended CMOS from which we select differential LVDS signals.

D. Controller unit

The entire data acquisition operation is controlled by the XC3S400 FPGA (Xilinx, 2007). It controls the memory block for write/read data by itself. The controller unit consists of Differential to Single-ended module (Xilinx, 2007), memory module and timing controller module. The block diagram of the controller unit is shown in Figure 3.

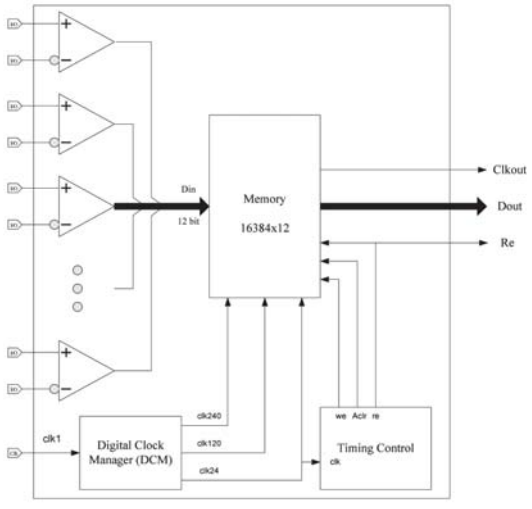

Figure 3. Block diagram of controller unit

Memory module use memory block which embedded in FPGA. The type of memory is FIFO (First In First Out). The memory size is 16384x12 bits. The memory need to record data at high speed rate. Hence this paper present memory which implement by two interlaced FIFO. Each FIFO size is 8192x12 bits as shown in Figure 4 below. The write process start at register1. The data is divided by Demultiplexer block in order to half speed of data rate. After that the data is recorded in memory ram1 and ram2. The read process are a mirror of the write process. The data from ram1 and ram 2 is multiplexed and passed to the register2 before it is output.

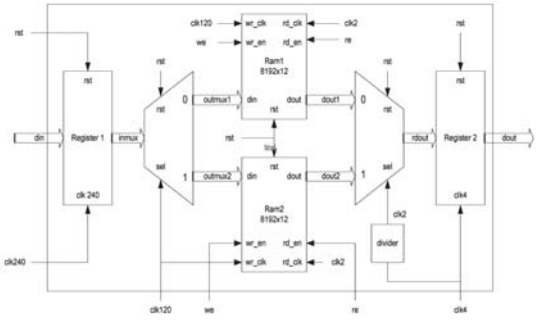

Figure 4. The structure of memory

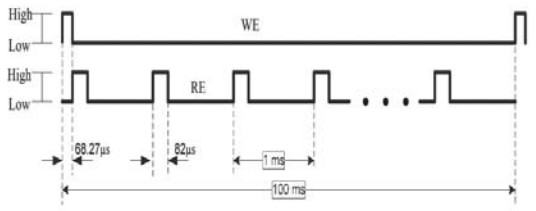

Figure 5. Timing diagram of the controller module

Timing controller module is implemented in VHDL code. This module control timing for write/read data in/out memory. Due to the sampling rate of 240 MSPS, the time used for storing 16384 samples is 68.27 ±s. The duration of data reading depends on read frequency. According to the full-speed USB specification, a PC read only 164x12 bits, and read again every millisecond. The timing for writing/reading of the controller module is shown in Figure 5.

E. USB Controller

The USB interface is implemented by a USB controller, embedded in a microcontroller. LPC2148 (Maxim, 2007) is selected for this purpose.

The LPC2148 USB is a full-speed device. The operation of the USB device driver can be simply defined in three phases: reset, enumeration, and finally, operation phase. The structure of USB data flow is shown in Figure 6.

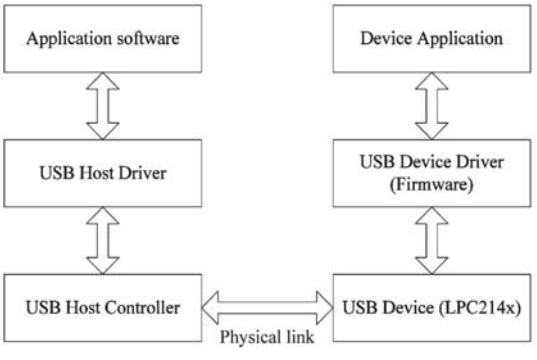

Figure 6. The structure of USB data flow

The software

The software is divided in 2 parts. The first part is firmware that is executed by the microcontroller. A simplified flowchart of operation is shown in Figure 7. The firmware starts with initialization of system clock and USB configuration. After that it makes USB connection and waits for an interrupt. If it occurs at the beginning of 1ms period, the microcontroller will send data to the host. Otherwise, it will check whether read signal is active. If so, it will update its data, which is sent from the FPGA. Otherwise, it will wait for next interrupt.

The second part is application software, which executed on a PC. A simplified flowchart of application software is shown in Figure 8. The application starts with checking whether user has clicked connect button. When the button is pressed and USB device is opened, the on status will be display. Otherwise, the off status will be display and back to the start. After, the on status is displayed and the Run button is pressed. The timer will start and wait until the time lapses 1ms, the application software will read and display data every millisecond.

Simualtion and Experimental result

The first experiment tests the LNA. When we insert 200 mV, 120MHz sinusoidal signal to LNA, output power is 2,000mW or 33dBm. In Figure 9, we show output frequency spectrum and Harmonic distortion at each order. The figure shows the fundamental power is 34.34dBm, the harmonic distortion at 2^{nd} and 3^{rd} are less than that 25.24dBc and 24.46dBc respectively.

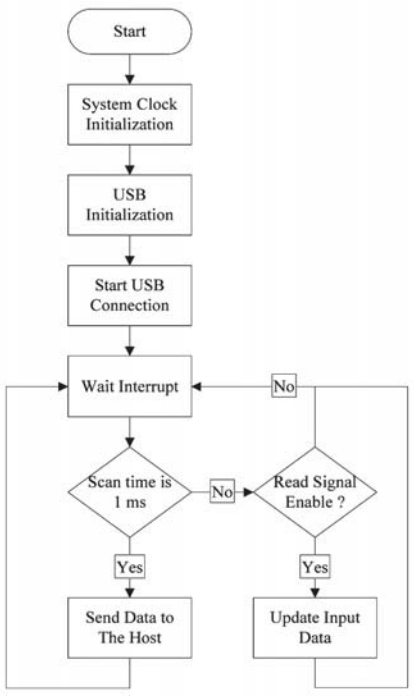

Figure 7. The frimware flowchart

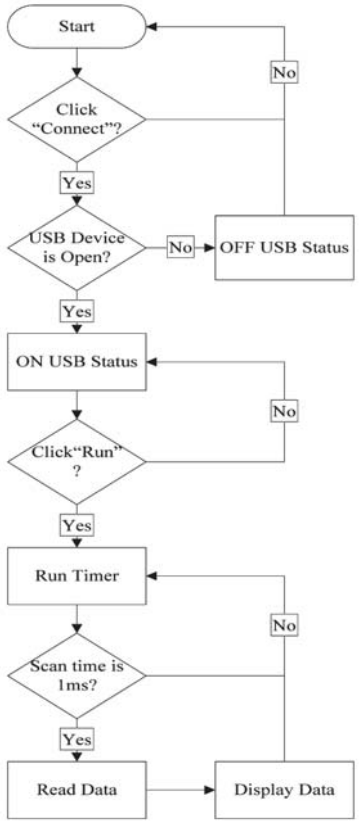

Figure 8. The application software flowchart

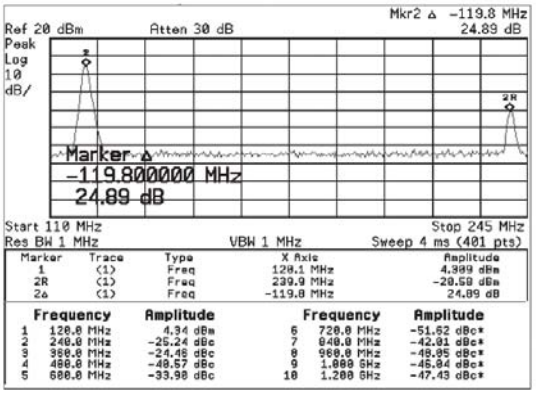

Figure 9. The frequency spectrum and harmonic distortion

The timing controller module controls write and read signal. They are represented by "WE" and "RE" respectively. The captures of oscilloscope screens are shown in Figure 10.

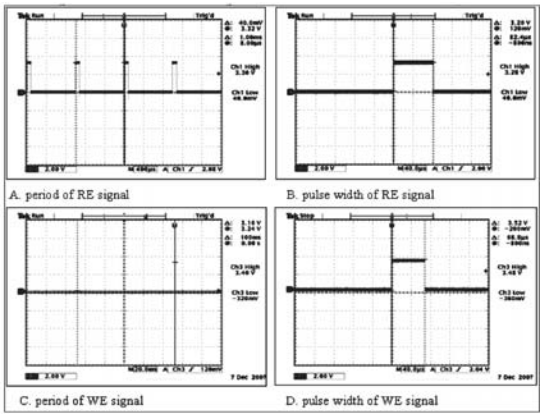

Figure 10. The timing control write/read data

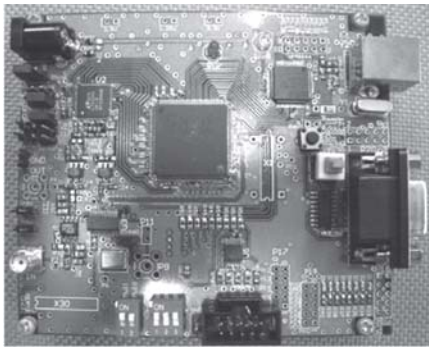

Figure 11. The Data Acquisition Board

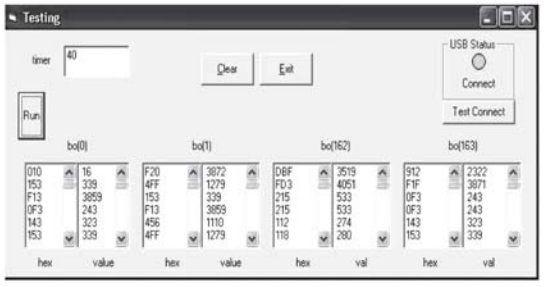

Figure 12. The application software window

Figure 11 shows 4-layer DAQ board. The board size is 3.5x4 inch. All high speed devices are on top layer.

Figure 12 shows application software window. It is developed with Microsoft Visual Basic 6.0. The application software display status of USB connection and data read from USB device. A frame of 246 byte data (equivalent to 164 samplings of 12bit data) is read by triggering of timer control. The triggering period is 1ms. After the data is read, it will display in the textbox control. Only sampling 0, 1, 162 and 163 are shown in Figure12.

Conclusion and development

Since analyses of the signal from HDD head is needed, and such signal has very small amplitude and high bandwidth, this paper presented development of a data acquisition board with an LNA and a high-speed ADC. It communicates with a PC via a USB port.

Although this data acquisition board has some good features, further development may be useful. A direction may include even higher sampling rate, higher amplification gain, or bigger memory size. This may impose a software/hardware modification of the entire system but it will increase the system flexibility.

Acknowledgment

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